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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,348	10/23/2003	Jeong-Seok Lee	5000-1-461	8525
33942	7590	04/07/2005	EXAMINER	
CHA & REITER, LLC 210 ROUTE 4 EAST STE 103 PARAMUS, NJ 07652			DUPUIS, DEREK L	
			ART UNIT	PAPER NUMBER
			2883	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/692,348

Applicant(s)

LEE ET AL.

Examiner

Derek L. Dupuis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The disclosure is objected to because of the following informalities: the sentence that begins on page 6, line 20 with "The optical power equalizer ..." does not read properly. Specifically, the period after the reference number 50 seems to be misplaced and the line "... to the OLT 50 to the optical power equalizer 100 allow ..." reads awkwardly. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Gentzler et al (US 6,396,344 B1)* in view of *Yoshida et al (US 6,437,320 B1)*.

5. Regarding claims 1 and 6, Gentzler et al teach an optical power equalizer and a method of optical power equalization as shown in claim 3 comprising a wavelength coupler (101) for separating an optical signal traveling upstream from an optical fiber. The equalizer is used in a TDMA transmission system that contain various signal

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components with different amplitudes (see column 2, line 63 to column 4, line 3) from various subscribers (ONU's) (see column 1, lines 5-21). The equalizer also includes a delay element (112) for delaying the upstream signal by a time required for a control signal to arrive at a desired location (see column 11, lines 27-37).

6. Gentzler et al teach that the control signal for which the upstream signal is delayed is an error correction signal that arrives at an amplifier (106), rather than a control signal for an amplifier. Furthermore, Gentzler et al do not teach an optical splitter to transfer a portion of the upstream signal to a detector that outputs an electrical signal having an amplitude proportional to the optical signal's intensity or an active gain control circuit for controlling a driving current, in accordance with the electrical signal, that drives the amplifier so as to amplify the upstream signal with an amplification gain according to the driving current of the gain control circuit.

7. Yoshida et al teach an optical amplifier and optical amplification control system as shown in figure 2. The system includes an optical splitter (122) to allow part of an upstream optical signal to be transferred to an optical detector (126) for detecting the signal's intensity. The optical detector (126) outputs an electrical signal having a signal amplitude proportional to the upstream optical signal's intensity (see column 4, lines 5-12). Yoshida et al also teach an active gain control circuit (130) for controlling a driving current to be provided to an optical amplifier in accordance with the electrical signal from the detector (126). The upstream optical signal is amplified with an amplification gain according to the driving current of the gain control circuit (see column 4, lines 5-20). The optical amplifier used by Yoshida et al is a laser diode pump (114) coupled to an optical fiber loop (118).

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8. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the TDMA system of Gentzler et al with the gain control system taught by Yoshida et al for the purpose of maintaining the flatness of the intensity of the time-multiplexed systems (see column 2, lines 1 and 2 of Yoshida et al) and to keep the difference in power of different signals very small (see column 1, lines 51-55 of Yoshida et al).

9. Regarding claim 3, Gentzler et al in view of Yoshida et al teach an optical power equalizer as discussed above in reference to claim 1. Yoshida et al teach a semiconductor optical amplifier (see column 1, lines 25-31 of Yoshida et al). The laser pump is a semiconductor laser.

10. Regarding claims 4 and 7, Gentzler et al in view of Yoshida et al teach an optical power equalizer and a method for optical power equalization as discussed above in reference to claims 3 and 6, respectively. Gentzler et al teach that the system operates at 100 GHz which would mean the switching time of the optical amplifier would have an order of magnitude of nanoseconds (see column 11, lines 46-50 of Gentzler et al). The delay step would also have an order of magnitude of nanoseconds.

11. Regarding claim 5, Gentzler et al in view of Yoshida et al teach an optical power equalizer as discussed above in reference to claim 1. Yoshida et al teach that the driving current from the active gain control circuit has an amplitude that is inversely proportional to the intensity of the upstream optical signal. If the signal is too small, the driving current amplitude is large (see column 4, lines 23-40 of Yoshida et al).

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12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Gentzler et al (US 6,396,344 B1)* in view of *Yoshida et al (US 6,437,320 B1)* as applied to claim 1 above, and further in view of *Chow et al (US 2002/0145776 A1)*.

13. Regarding claim 2, Gentzler et al in view of Yoshida et al teach an optical power equalizer as discussed above in reference to claim 1. While Gentzler et al teach a delay device, Gentzler et al nor Yoshida et al explicitly state that the delay device is a fiber loop. Chow et al teach the use of a fiber loop to create a delay. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the power equalizer of Gentzler et al by using a fiber loop as a delay as taught by Chow et al for the purpose of “manufacturing a time delay in the nanosecond to microsecond range to enable a supporting electrical function time to perform its tasks” (see paragraph 12 of Chow et al). Furthermore, fiber loops are well known delay devices in the art of optical communication.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derek L. Dupuis whose telephone number is (571) 272-3101. The examiner can normally be reached on Monday - Friday 8:30am-4:30pm.

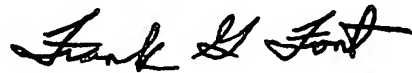
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Derek L. Dupuis
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Frank G. Font
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